SPECIFICATION

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[BUMP LAYOUT ON SILICON CHIP]

Cross Reference to Related Applications

This application claims the priority benefit of Taiwan application serial no. 90119108, filed on 2001/8/6.

Background of Invention

[0001] Field of Invention

[0002] The present invention relates to a bump layout on a silicon chip. More particularly, the present invention relates to a bump layout on a silicon chip such that pressure is distributed evenly to each bump and maximum permissible pitch is retained between the edges of neighboring bumps to reduce the probability of a short circuit.

[0003] Description of Related Art

[0004] Due to rapid progress in semiconductor device and display device fabrication, multi-media communication is becoming increasingly popular. Although cathode ray tube (CRT) displays can provide relatively high image quality at a low cost, thin film transistor (TFT) liquid crystal display (LCD) devices are gradually replacing CRTs because the TFT LCD is thinner and consumes less power. However, aside from a liquid crystal display panel, a LCD display also needs a driver IC to drive the display panel. In recent years, the demand to display a huge volume of data has jacked up the total number of input/output (I/O) terminals needed on a liquid crystal panel driver. For example, a driver IC having 308, 309, 384 or even 420 input/output terminals is quite common. In addition, the driver IC must correspond in size with the liquid crystal display panel. Hence, the driver IC often has a rectangular plan so that the number of I/O pads along the edges of the driver IC is maximized. Typically, a driver

chip and a liquid crystal display panel are joined together in a chip-on-glass (COG) process, a chip-on-film (COF) process, a chip-on-board (COB) process or a tape-automated-bonding (TAB) process.

[0005] In a chip-on-glass (COG) method, the bumps on the driver IC are positioned according to the configuration. In a gate driver IC configuration, the total number of input/output terminals is smaller. However, in a source driver IC configuration, the driver IC has more input/output terminals.

[0006] Fig. 1 is a top view showing the bump layout of a conventional LCD driver IC. In general, the bumps 102 of a driver IC 100 of most super-twist-oriented LCD (STN-LCD) or TFT-LCD are arranged as a single row along the edges surrounding the active area of the driver IC 100. In other words, the bumps enclose an area on the driver IC 100 containing a circuit 104.

[0007] As shown in Fig. 1, the bumps are principally positioned along the edges of the driver IC with the central region reserved for housing the circuits. Since the bumps are placed along the edge in a single file, the maximum number of bumps that can be laid depends on overall peripheral length of the driver IC, size of each bump and pitch between neighboring bumps. Hence, the only way to increase the number of bumps on the driver IC having this type of layout is to shrink the bumps.

[0008] Fig. 2 is a top view showing bump layout of a conventional TFT LCD driver IC. As shown in Fig. 2, the total number of bumps 202 on the driver IC 200 is considerably greater than the total number of bumps 102 on the driver IC 100 shown in Fig. 1. Due to the total number of bumps required on the driver IC 200 and consideration regarding the dimensions of the liquid crystal display, the source driver IC is designed to have a narrow rectangular structure. The central area of the driver IC 200 encloses an active region or a circuit region 204. Bumps 202 close to a first edge 206 on one side of the active region 204 are positioned alternately on two rows. Bumps close to a second edge on the opposite side of the active region 204 are positioned in a single row. Furthermore, bumps 202 close to a first short side 210 and a second short side 212 of the driver IC are positioned in an array format.

[0009] The bumps 202 on the conventional source driver IC 200 as shown in Fig. 2 are

unevenly distributed. In COG manufacturing, this non-uniform bump layout may produce an uneven stress around the peripheral region of the driver IC 200. Thus, fewer cracks will form close to the short edges 210 and 212 and more cracks will form elsewhere. Ultimately, reliability of the assembled structure is compromised.

Summary of Invention

[0010] Accordingly, one object of the present invention is to provide a bump layout that facilitates the placement of more bumps on the active region of a driver IC and the optimization of pressure distribution in chip-on-glass manufacturing. Hence, lighter marks on the shorter sides of a conventional rectangular drive chip are prevented.

[0011] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a bump layout on a driver IC. The bumps are arranged to form a grid array over the active region of the driver IC. The bumps, for example, may be spread out in a regular array, in alternating non-aligned rows, or a mixture of the two. One principal criterion in the bump layout is to spread out all the bumps as evenly as possible so that equal pressure is conferred to each bump in chip-on-glass manufacturing. Circuits of the driver IC are formed underneath the bump space region, the area between the bumps. Hence, driver IC area is more effectively utilized and the driver IC may include more bumps.

[0012] This invention also provides a bump layout on a driver IC. The bumps are laid out in a manner on the driver IC such that no bumps are located over regions with light marking pressure. Since a thin film transistor (TFT) liquid crystal display (LCD) package has a narrow rectangular profile, the driver IC has a first long side, a second long side, a first short side and a second short side. Bumps are positioned over the active area of the driver IC according to a few layout strategies. Bumps close to the first long side of the driver IC package are laid in alternating non-aligned rows. Bumps close to the second long side of the driver IC package are laid in a single row. No bumps are laid in the neighborhood of the first short side or the second short side. Those bumps close to the shorter sides of a conventional driver IC package are shifted towards more central regions so that lighter marking pressure during COG manufacturing is prevented. A few dummy bumps may be introduced into the

neighborhood of the shorter sides after moving bumps close to the shorter sides towards the central region. Since the aforementioned bump layout may divide the active region into several circuit blocks, the circuit blocks may be connected with each other by forming special circuit lines.

[0013] Dummy bumps may also be introduced close to the first short side and the second short side of the driver IC package so as to balance out the pressure on a source driver IC during COG manufacturing.

[0014] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0015] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0016] Fig. 1 is a top view showing bump layout of a conventional LCD driver IC;

[0017] Fig. 2 is a top view showing bump layout of a conventional TFT LCD driver IC;

[0018] Figs. 3 and 4 are top views showing two alternative bump layouts of a driver IC according to a first preferred embodiment of this invention;

[0019] Fig. 5 is a top view showing bump layout of a driver IC according to a second preferred embodiment of this invention; and

[0020] Fig. 6 is a top view showing bump and dummy bump layout on a driver IC according to a fourth preferred embodiment of this invention.

Detailed Description

[0021]

Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to

refer to the same or like parts.

[0022] Figs. 3 and 4 are top views showing two alternative bump layouts of a driver IC according to a first preferred embodiment of this invention. To match the ever-increasing demand for input/output (I/O) terminals in a driver IC package, the driver IC 300 of this invention is able to provide more bumps 302 in the active region. As shown in Fig. 3, the bumps 302 are positioned to form a grid array in the active region. The bumps are arranged, for example, to form a vertically aligned grid over the active region so that pressure is evenly distributed during chip-on-glass (COG) manufacturing. Circuit regions 304 are formed underneath bump space between neighboring bumps. Thus, surface area of the driver IC 300 is fully utilized so that more bumps 302 may fit into the driver IC package.

[0023] Similarly, the bumps 402 in Fig. 4 are positioned to form a grid array in the active region. However, the bumps are positioned along alternating non-aligned or staggered rows over the active region so that pressure is more evenly spread out over the driver IC 400 during COG manufacturing. Circuit regions 404 are formed underneath bump space between neighboring bumps 402. Therefore, surface area of the driver IC 400 is fully utilized so that more bumps 402 may fit into the driver IC package. Furthermore, a bump layout having a mixture of the vertically aligned grid and the alternating non-aligned row pattern is permissible depending on actual requirements.

[0024] Whatever the type of array format (grid type or alternative non-aligned row pattern) selected, more bumps may be fitted inside the driver IC package for identical bump size and bump pitch. Ultimately, the bump space between the edges of neighboring bumps is unaffected by side length of the driver IC.

[0025] Fig. 5 is a top view showing bump layout of a driver IC according to a second preferred embodiment of this invention. As shown in Fig. 5, the driver IC 500 has an active region with four sides including a first long side 506, a second long side 508, a first short side 510 and a second short side 512. Bumps 502 close to the first long side 506 of the active region are positioned to form, for example, two alternative non-aligned rows. Bumps 502 close to the second long side 508 of the active region are positioned to form, for example, a single row. No bumps are laid within the region

close to the first short side 510 or the second short side 512. In this embodiment, bumps close to the shorter sides of a conventional driver IC are moved towards the central region of the driver IC package. With this arrangement, light marking pressure on the first shorter side 510 and the second shorter side 512 during chip-on-glass (COG) manufacturing is prevented. Due to the aforementioned bump layout, circuit regions 504 are divided into several sub-circuit blocks 504a, 504b and 504c. However, these sub-circuit blocks may be linked together by forming circuit lines.

[0026] Fig. 6 is a top view showing bump and dummy bump layout on a driver IC according to a fourth preferred embodiment of this invention. The bump layout in Fig. 6 is very similar to the bump layout shown in Fig. 5. Bumps 602 close to the short sides (610 and 612) of a conventional driver IC package are also moved to a more central region of the driver IC package so that light marking pressure during COG manufacturing is prevented. However, dummy bumps 606 are also formed in the active region close to the first short side 610 and the second short side 612. In subsequent COG manufacturing operations, the dummy bumps 606 on the driver IC 600 are able to even out pressure distribution. In addition, even if light marking pressure occurs in subsequent COG manufacturing, bondage between the driver IC and glass is unaffected because the dummy bumps 606 have no electrical connection with external circuits.

[0027] Although the bump layout is explained using gate driver IC and source driver IC as example, the bump layout according to this invention has a wide spectrum of applications including COG, COF, COB and TAB manufacturing of an IC chip.

[0028] In conclusion, major advantages of the bump layout according to this invention includes:

[0029] 1. More bumps are packed inside a driver IC.

[0030] 2. The bump layout is able to equalize pressure distribution in many types of manufacturing including COG, COF, COB and TAB.

[0031] 3. Light marking pressure on the short sides of a driver IC is eliminated after a COG, COF, COB or TAB manufacturing operation so that electrical connections are unaffected.

[0032] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.